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12EC126

M.Tech. Degree Examination, June/July 2013
Real Time Operating Systems

Time: 3 hrs. Max. Marks:100

Note: ***1. Answer any FIVE full questions.***
2. Write diagrams, examples and illustrations, wherever necessary.

1 a. Write the flowchart and the pseudocode for a basic real time service using polling technique. What are the changes to be done in the pseudocode if the count-driven service is to be provided? **(12 Marks)**

b. Draw the timeline for RTS and define the various terms. What are the advantages of hardware acceleration? Show the changes in the RTS timeline with H/W acceleration. **(08 Marks)**

2 a. Describe the six real time service utility functions with graphs and examples. **(12 Marks)**

b. Write the state transition diagram and state transition table for a thread of execution including all possible states. **(08 Marks)**

3 a. Derive the equation for RMLUB considering two services with two different cases. Write only the timing diagram for the 2 cases and the relationship to T_2 and T_1 pictorially no other graphs are required. **(12 Marks)**

b. Distinguish between:
i) Scheduling point test and completion time test.
ii) RM and DM policies for scheduling. **(08 Marks)**

4 a. Briefly describe the following terms:
i) Pipelining technique.
ii) Physical memory hierarchy and
iii) Flash file systems. **(12 Marks)**

b. Show the scheduling pattern for the two dynamic priority policies with timing diagram and the values or priorities calculated at each preemption for the following case: There are 3 services with $T_1 = 2$ secs, $T_2 = 5$ secs, $T_3 = 7$ secs, $C_1 = 1$ sec, $C_2 = 1$ sec and $C_3 = 2$ seconds. What is the utilization of the CPU and RMLUB? **(08 Marks)**

5 a. Describe ECC memory logic design when data byte = $(1\ 1\ 0\ 0\ 0\ 1\ 0\ 0)_2$. Assume that 10^{th} bit (d06) has changed/flipped to 0 from 1, in the encoded data bit stream. Show how the single bit error is detected and can be corrected using ECC logic. Write totally 3 tables for showing the design and error detection. **(12 Marks)**

b. Describe deadlock and critical section with shared memory as resource and the use of semaphores as a solution to this problem. **(08 Marks)**

6 a. Briefly explain the following terms:
i) Priority inversion
ii) Intermediate I/O and
iii) Quality of service. **(12 Marks)**

b. Determine the WCET, ACET and response time for job and availability value, if the parameters of the real time system are as follows: memory latency is 12 clock cycles, IO-latency is 60 clock cycles, NOA is 0.6, longest path instruction count is 2800, expected path instruction count is 2500, expected cache miss rate is 45%, cache miss penalty is 14 clock cycles, CPI effective for all the cases is 2, total interference time for job_i is 200 m seconds, clock frequency of the system is 40 MHz, MTBF is 5 hours and MTTR is 15 minutes deadline for job_i is 1600 m secs. Is it possible for job_i to finish the work before deadline, considering WCET and total interference time as its response time. **(08 Marks)**

7 a. Describe the 3 firmware components and any 3 RTOS system software mechanisms. **(12 Marks)**

b. Explain the following terms briefly:
i) Exceptions and asserts.
ii) Single-step debugging types. **(08 Marks)**

8 a. Describe:
i) Drill down tuning and
ii) Reliability, reliable software and available software. **(12 Marks)**

b. What are the issues to be considered for the design of RTOS using a PIC microcontroller.? **(08 Marks)**

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